ABSTRACT

According to an embodiment of the present invention, a microprocessor includes an expanded logical register set that can be accessed by instructions including legacy opcodes and remapped addressing mode information. The known IA-32 instruction set is limited to accessing eight logical general integer registers. An IA-32 instruction can specify which of the eight logical general integer registers are to be accessed via 3-bit register identifier fields of the addressing mode information of the instruction. Each 3-bit register identifier can specify any of the eight logical general integer registers. An expanded logical register set (e.g., sixteen logical registers, thirty-two logical registers, sixty-four logical registers, etc.) can be accessed by remapping the addressing mode information to include at least four-bit register identifiers without defining new opcodes or defining additional instruction prefixes.